A Diamond:H/MoO_3 MOSFET

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***Abstract*— A p-type MOSFET based on a heterointerface of hydrogenated-diamond transfer doped with MoO_3 (Diamond:H/MoO_3) is demonstrated for the first time. This is an important new heterostructure system due to its potentially improved temperature stability as compared with the better established Diamond:H/H_2O system. MOSFETs using HfO_2 as gate insulator show excellent output characteristics and gate control over the 2-D hole gas at the Diamond:H/MoO_3 interface. In 3.5-μm gate length devices, we obtain a maximum drain-current ON-OFF ratio of three orders of magnitude and a maximum transconductance of 2.5 μS/μm.**

***Index Terms*— Diamond:H, MoO_3, surface transfer doping, MOSFET.**

I. Introduction

DIAMOND is widely considered the ultimate semiconductor for the realization of unique solid-state microelectronics devices. This is thanks to its outstanding mechanical, electrical and thermal properties, such as extreme hardness, high breakdown electric field (>10 MVcm^{-1}), very high thermal conductivity (>20 W/cm·K) and high intrinsic carrier mobility at room temperature (μ_h = 3800 and μ_e = 4500 cm^2/V·s) [1].

Progress in the realization of diamond-based electronic devices has been hampered by the lack of suitable acceptors and donors with low activation energies. The most common dopants, B (p-type) and P (n-type), have activation energies of 0.37 eV and 0.6 eV, respectively [2]. This drawback has been partially overcome through the discovery of surface conductivity in hydrogen-terminated diamond (Diamond:H) [3]. This has been explained by a model that is known as "surface transfer doping" [4]. Surface transfer doping is achieved by exposing Diamond:H to different surface acceptors with high work function [5], [6]. Charge transfer between the diamond surface and the absorbed species takes place that leads to a highly conductive sheet of holes at the diamond sub-surface. The surface transfer doping system that has been most studied consists of Diamond:H exposed to H_2O molecules. This exhibits a two dimensional hole gas [7] with an aerial hole density of 5×10^{13} cm^{-2} and a mobility of several tens of cm^2/V·sec [8]. Using this system, field-effect transistors [9]–[12] and logic circuits [13] have been demonstrated.

A major difficulty of the Diamond:H/H_2O system is the gradual desorption of H_2O that takes place at even moderate temperatures (<200°C). This results in instabilities and loss of electrical conductivity [14] posing severe constraints on the process technology as well as the reliability of transistors fabricated in this system. Atomic Layer Deposition (ALD) of the gate oxide using H_2O precursor has recently ameliorated the situation [15] and MOSFETs fabricated by ALD have been shown to be stable up to 400°C under vacuum conditions [16]. Nevertheless, it would be desirable to identify a surface transfer diamond system that is intrinsically stable.

Recently, MoO_3 has been shown to exhibit excellent transfer doping properties with Diamond:H [17], [18], yielding the highest yet reported areal hole density (ranging from 7×10^{13} to 1×10^{14} cm^{-2}) and showing temperature stability up to at least 350°C under atmospheric ambient conditions and without an additional cap layer [18]. This makes this heterostructure system attractive for Diamond:H-based electron device that are fabricated through a flexible and robust process. In this letter, we report the first demonstration of a Diamond:H/MoO_3 transfer-doped MOSFET. While the performance is modest, opportunities for substantial device improvement clearly exist.

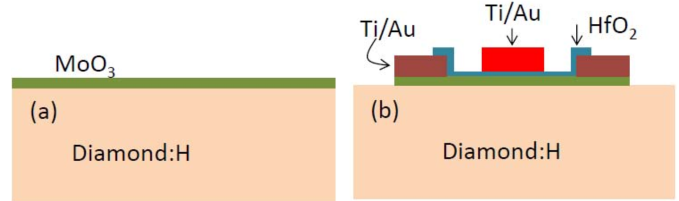

Fig. 1. Schematic of Diamond:H/MoO_3 p-type MOSFET: (a) starting heterostructure, (b) final device cross section.

II. Device Fabrication

Figure 1 show a schematic cross-sectional view of the starting heterostructure and the final device. The starting substrate is a commercially available $3 \times 3 \times 0.5$ mm^3 type IIa (001)-oriented single-crystal diamond. Surface hydrogenation was accomplished by exposure to pure hydrogen plasma in a CVD reactor at 600°C for 40 minutes.

Following surface hydrogenation, the sample was heated to 350°C to desorb any H_2O molecules and contaminants from the surface immediately after which (*in situ*) 4 nm of MoO_3 was thermally evaporated. In order to assess the chemical bonding and stoichiometry of the oxide, X-ray photoelectron

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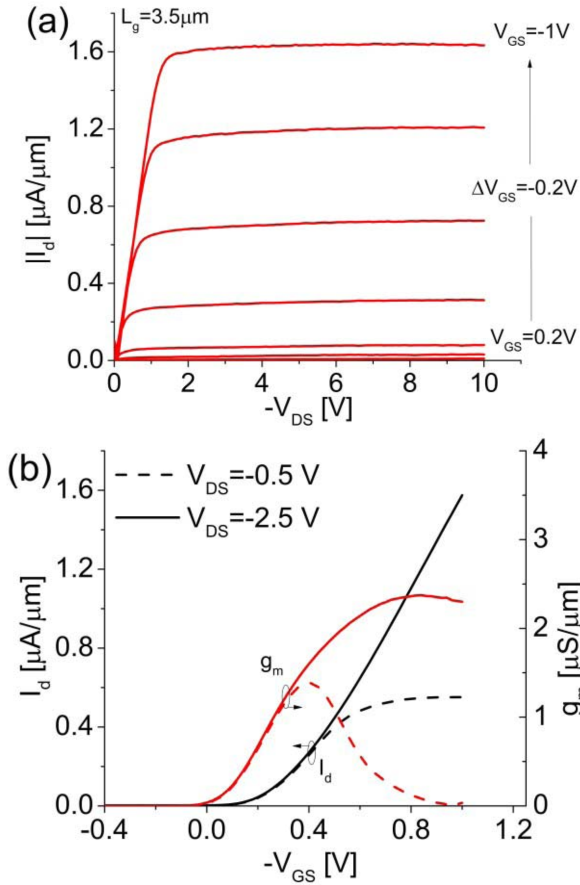

Fig. 2. Output (a) and transfer (b) characteristics of $L_g = 3.5\ \mu m$ Diamond:H/MoO_3 p-type MOSFET.

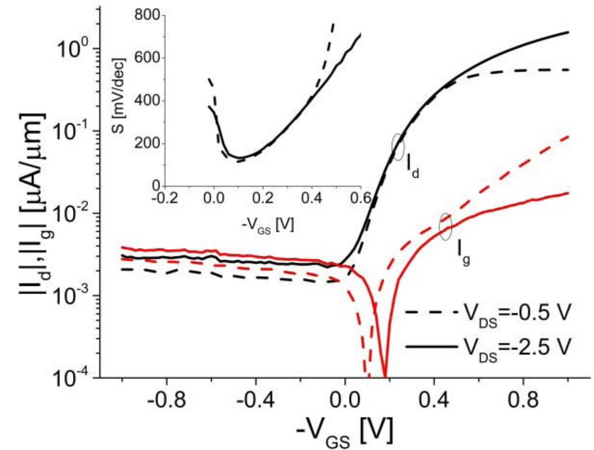

Fig. 3. Diamond:H/MoO_3 subthreshold and gate current characteristics and subthreshold swing (inset) of the MOSFET featured in Fig. 2.

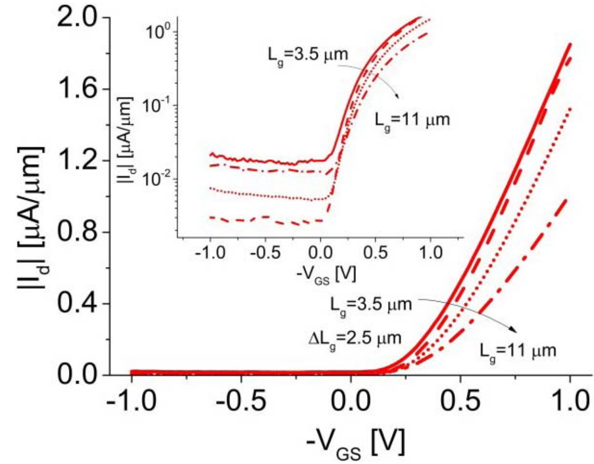

Fig. 4. Transfer and subthreshold (inset) characteristics at $V_{DS} = -2.5$ V for devices with different gate lengths.

spectroscopy (XPS) measurements of Mo3d core level spectra were carried out right after MoO_3 deposition [18]. The Mo^{6+} oxidation state was predominantly observed with only a small fraction (3–4%) of Mo^{5+} being present.

Device fabrication starts with mask definition for ohmic contacts followed by Ti/Au (20/200 nm) evaporation and liftoff. 10 nm of HfO_2 are then deposited by ALD at 200°C. HfO_2 was chosen as a gate oxide in order to protect the MoO_3 layer during a wet HF etch that is required later in the process. After HfO_2 deposition, flowable oxide (FOX) is spun on the sample surface. The FOX layer is exposed by electron-beam lithography and used as a hard mask to define the active area. RIE based on a BCl_3/Cl/Ar chemistry is used to etch the exposed HfO_2 and MoO_3 films. Device isolation was confirmed by electrical measurements and the FOX was then striped. Following a standard photolithography step, a Ti/Au (20/200 nm) gate was lifted off. Devices with gate lengths (L_g) ranging from 3.5 to 11 μm were fabricated. For all devices, the source- and drain-to-gate separation is 2 μm.

III. Results

Fig. 2 shows electrical characteristics of a typical MOSFET with $L_g = 3.5\ \mu m$. The output characteristics in Fig. 2a show excellent drain current saturation and low output conductance.

The transfer characteristics in Fig. 2b indicate a broad transconductance peak. g_{m_max} is 2.3 $\mu S/\mu m$ and V_t, defined at 0.1 $\mu A/\mu m$, is 0.2 V. The subthreshold and gate characteristics for the same device are shown in Fig. 3. They indicate negligible DIBL and a minimum subthreshold swing of 100 mV/dec. This is likely to be an upper limit since the OFF current is limited by relatively large gate leakage current. The ON-OFF current ratio for this device is 3 orders of magnitude.

Fig. 4 shows transfer and subthreshold characteristics (inset) at $V_{DS} = -2.5$ V of devices with different gate lengths from 3.5 to 11 μm. The ON current scales up as L_g is reduced. A variation in V_t of about 50 mV is observed although no systematic dependence on L_g was found.

The low drain current density of these first prototype devices is greatly affected by their large parasitic resistance. In order to estimate the ON resistance under conditions of substantial gate leakage current, we averaged the source and drain currents at low V_{DS}. This is done under the assumption that the device is symmetric and that for low drain bias the contribution of the source and drain terminals to the gate leakage current is roughly equal. From these measurements, we estimate an

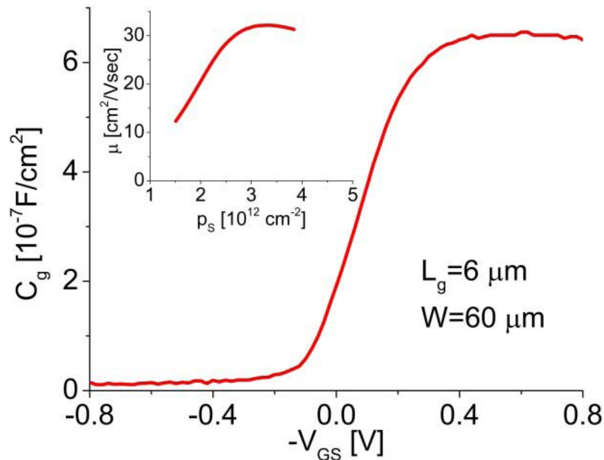

Fig. 5. Split C-V measurements at 1 MHz of a typical device. Inset: hole mobility vs. sheet hole concentration obtained from C-V and I-V data for the same device.

average channel sheet resistance of 140 kΩ/□ and an access resistance (assuming $R_s = R_d$) of 185 kΩ-μm.

The linearity of the output characteristics for small V_{DS} confirms that the contacts are ohmic. Nevertheless, the access resistance that we measure is about an order of magnitude higher than the typical Ti/Au - Diamond:H contact resistance [19]. This most likely is the result of having left the MoO_3 layer underneath the contact metal which was done with the goal of minimizing any disturbance to the transferred layer doping in that region. Future research will be dedicated to mitigating this problem.

To further understand the operation of these devices, the gate capacitance-voltage characteristics were measured at high frequency (1 MHz). A typical result is shown in Fig. 5. The CV characteristics show classic MOSFET behavior. The extracted EOT is 5.2 nm which is consistent with the nominal oxide thicknesses of the MoO_3 and HfO_2 films (given above) and their respective permittivities (6 and 18, as commonly given). The combination of C–V and I–V characteristics in the linear regime enables the extraction of the hole mobility and sheet hole concentration. For this we have corrected the gate leakage current and used an estimate of the access resistance extracted from L_g extrapolation. The inset in Fig. 5 shows μ vs. p_s. The obtained maximum sheet carrier concentration and mobility are 4×10^{12} cm^{-2} and 30 cm^2/V·sec. These results are somehow lower than expected for the given MoO_3 layer thickness [18]. This is attributed to MoO_3 reduction during the device fabrication process which affects the oxidation state and reduces its work function [20].

While the characteristics of this device are modest, with adequate precautions to protect the MoO_3 surface during processing and eliminating it under the contacts, we expect the device performance to improve substantially.

IV. Conclusion

We demonstrate for the first time a Diamond:H/MoO_3 p-type MOSFET. We show classic I–V and C–V MOSFET characteristics. In spite of the process technology reaching 200°C, stable transistor operation was obtained.

Acknowledgment

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